LISTING OF CLAIMS:

1. (currently amended): A computer system, comprising:

a first cluster including a first processor and a second processor of a first plurality of processors and a first interconnection controller, ~~the first plurality of processors and the first interconnection controller in communication using a point-to-point architecture~~wherein the first processor is connected to the second processor through a point to point link and the first processor is connected to the first interconnection controller through a point to point link and the second processor is connected to the first interconnection controller through a point to point link;

a second cluster including a second plurality of processors and a second interconnection controller, the second plurality of processors and the second interconnection controller in communication using a point-to-point architecture, wherein disabling the second cluster comprises disabling polling for a link from the first interconnection controller to the second interconnection controller ~~can be enabled or disabled by configuring the first interconnection controller~~and flushing caches associated with the second cluster.

2. (original): The computer system of claim 1, wherein the first cluster of processors and the second cluster of processors share a single virtual address space.

3. (original): The computer system of claim 1, wherein the first interconnection controller includes a physical layer enable indicator.

4. (original): The computer system of claim 1, wherein the first interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller.

5. (original): The computer system of claim 1, wherein the first interconnection controller includes a reinitialization indicator configurable to direct the first interconnection controller to reinitialize the link.

6. (original): The computer system of claim 5, wherein reinitialization comprises having a transmitter associated with the first interconnection controller send a training sequence to the second interconnection controller.

7. (original): The computer system of claim 6, wherein the transmitter sends the training sequence when the polling active state is set.

8. (original): The computer system of claim 7, wherein the transmitter does not sent the training sequence when the polling sleep state is set.

9. (original): The computer system of claim 5, wherein reinitialization comprises having a associated with the first interconnection controller send an initialization sequence to the second interconnection controller.

10. (original): The computer system of claim 1, wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors.

11. (original): The computer system of claim 1, wherein the first interconnection controller includes configuration space registers comprising physical layer enable, fence, reinitialization, and cluster ID bits.

12. (currently amended): A method for introducing a cluster of processors, the method comprising:

configuring a first interconnection controller in a first cluster including a first plurality of processor in communication using a point-to-point architecture to poll for the presence of a second interconnection controller;

asserting a reset signal on a second interconnection controller in a second cluster including a second plurality of processors in communication using a point-to-point architecture;

establishing, after asserting the reset signal, a link layer protocol on a connection between the first and second interconnection controllers.

13. (original): The method of claim 12, wherein polling is performed continuously.

14. (original): The method of claim 12, wherein the first interconnection controller includes a physical layer enable indicator.

15. (original): The method of claim 12, wherein the first interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller.

16. (original): The method of claim 12, wherein the first interconnection controller includes a reinitialization indicator configurable to direct the first interconnection controller to reinitialize the link.

17. (original): The method of claim 16, wherein reinitialization comprises having a transmitter associated with the first interconnection controller send a training sequence to the second interconnection controller.

18. (original): The method of claim 17, wherein the transmitter sends the training sequence when the polling active state is set.

19. (original): The method of claim 18, wherein the transmitter does not sent the training sequence when the polling sleep state is set.

20. (original): The method of claim 16, wherein reinitialization comprises having a associated with the first interconnection controller send an initialization sequence to the second interconnection controller.

21. (original): The method of claim 12, wherein the first interconnection controller includes a plurality of cluster ID indicators operable to hold values identifying remote clusters of processors.

22. (original): The computer system of claim 12, wherein the first interconnection controller includes configuration space registers comprising physical layer enable, fence, reinitialization, and cluster ID bits.

23. (currently amended): A computer system, comprising:

means for configuring a first interconnection controller in a first cluster including a first plurality of processor in communication using a point-to-point architecture to poll for the presence of a second interconnection controller;

means for asserting a reset signal on a second interconnection controller in a second cluster including a second plurality of processors in communication using a point-to-point architecture;

means for establishing, after asserting the reset signal, a link layer protocol on a connection between the first and second interconnection controllers.

24. (original): The computer system of claim 23, wherein polling is performed continuously.

25. (original): The computer system of claim 23, wherein the first interconnection controller includes a physical layer enable indicator.

26. (original): The computer system of claim 23, wherein the first interconnection controller includes a fence indicator configurable to prevent the transmission of logical packets between the first interconnection controller and the second interconnection controller.

27. (original): The computer system of claim 23, wherein the first interconnection controller includes a reinitialization indicator configurable to direct the first interconnection controller to reinitialize the link.

28. (original): The computer system of claim 27, wherein reinitialization comprises having a transmitter associated with the first interconnection controller send a training sequence to the second interconnection controller.

29. (original): The computer system of claim 28, wherein the transmitter sends the training sequence when the polling active state is set.

30. (original): The computer system of claim 29, wherein the transmitter does not sent the training sequence when the polling sleep state is set.

31. (original): The computer system of claim 27, wherein reinitialization comprises having a associated with the first interconnection controller send an initialization sequence to the second interconnection controller.